# 2–19-GHz Low-DC Power and High-$IP_3$ Monolithic HBT Matrix Amplifier

K. W. Chang, B. L. Nelson, A. K. Oki, and D. K. Umemoto

*Abstract*— **The design and performance of the first wide-band, low-dc power and high-$IP_3$ monolithic matrix amplifier using GaAs/AlGaAs heterojunction bipolar transistors (HBT's) is reported. The amplifier uses four $2\times10$ $\mu m^2$ quad-emitter HBT's in a $2\times2$ matrix configuration and has a measured gain of 9.6 ± 0.9 dB over the 2–19-GHz frequency band. Measured output $IP_3$ and 1-dB compression point are 26 dBm and 13 dBm, respectively, at 18 GHz. The total dc-power dissipation is less than 200 mW. The input and output return losses are better than –9.5 dB within the 2–16-GHz bandwidth.**

## I. Introduction

WIDE-BAND HBT monolithic amplifiers based on both distributed and Darlington feedback designs have been reported [1]–[3]. The first monolithic HBT distributed amplifier (DA) used four $3\times10$-$\mu m^2$ single-emitter self-aligned base ohmic metal (SABM) devices and achieved 6–10-dB gain for frequencies up to 9 GHz. This DA had an output 1-dB compression point of 7 dBm [1]. The first low-dc power dissipation matrix amplifier using three $2\times6$-$\mu m^2$ and three $2\times10$-$\mu m^2$ single-emitter devices with advanced device doping profiles allowed the 3-dB bandwidth to increase to 24 GHz [2]. The $IP_3$ and 1-dB compression point of this amplifier were predicted to be low due to the small-size devices used in the design. This letter reports a 2–19-GHz high $IP_3$ monolithic matrix amplifier with a nominal gain of 9.6 dB. Measured $IP_3$ and 1-dB compression point of the amplifier are more than 22 dBm and 9 dBm, respectively, for the entire frequency range.

## II. Circuit Design

The design procedure for a matrix amplifier is similar to that for the DA [4]. Since the bandwidth performance of a HBT DA is limited primarily by the input capacitance of the device, two common techniques, i.e., device scaling and capacitive coupling, have been utilized to reduce the device input capacitive and increase the amplifier bandwidth [5]. The capacitance coupling technique combined with the use of larger devices was used in the current amplifier design to increase the bandwidth and achieve a high 1-dB compression point as well as $IP_3$. The circuit schematic of the monolithic matrix amplifier is shown in Fig. 1. A total of four identical $2\times10$-$\mu m^2$ quad-emitter HBT's were implemented in the form of a $2\times2$ matrix. Each tier in the matrix is a DA structure consisting of two HBT's connected by microstrip transmission lines and terminated with resistive loads. Each HBT device has a capacitor of 0.3–0.5 pF in series with the base input lines and two resistors for self-biasing. The design goal was to achieve a broad-band, general purpose high-$IP_3$ amplifier with 10-dB gain and minimum dc power requirement. When compared to a DA that consists of two two-stage DA's in cascade, the matrix amplifier design is more compact and has more gain in the higher frequency band. One disadvantage of this design approach is, however, the poor noise performance at low frequencies due to the small input series capacitors, which provide a nearly open circuit to the devices at those frequencies. The device model and noise parameters of a $2\times10$-$\mu m^2$ quad-emitter HBT were reported in [1]. Fig. 2 is the photograph of the $2.5\times2.5$-$mm^2$ monolithic matrix amplifier chip including all the bias networks.

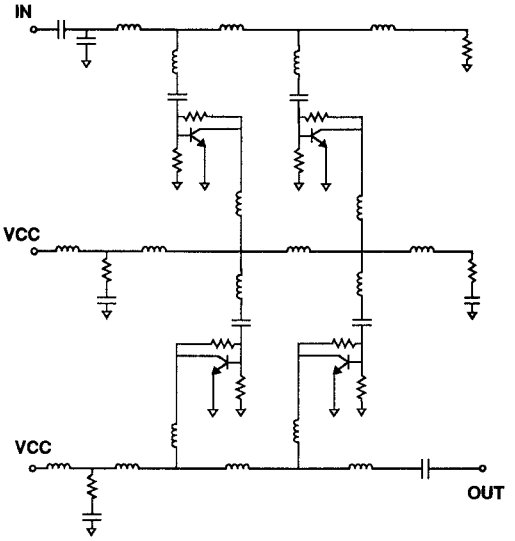


Fig. 1. Circuit schematic of the 2 × 2 matrix amplifier.

## III. Amplifier Performance

The matrix amplifier was biased at 3V and 64 mA. Total dc-power consumption is about 200 mW. Fig. 3(a) shows the measured results of amplifier gain, and the input and output return losses. The amplifier has a nominal gain of 9.6 dB and is unconditionally stable. The amplifier $IP_3$ and 1-dB compression point are illustrated in Fig. 3(b). The output 1-dB compression and $IP_3$ of the amplifier at 18 GHz are approximately 13 dBm and 26 dBm, respectively. These are the highest reported results at 18 GHz for an ultra broad-band

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The authors are with TRW, Electronics and Technology Division, One Space Park, Redondo Beach, CA 90278.

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TABLE I
SUMMARY OF THE BROAD-BAND HBT AMPLIFIERS

| Bandwidth | Gain (dB) | dc Power | $P_{1dB}$ @ GHz | Device $f_t$ | Ref. |
|---|---|---|---|---|---|
| 0.1–10 GHz | 8.0 ± 2.0 | ~60 mW | 7 dBm @ 10 | 23 GHz | DA [1] |
| 2–24 GHz | 9.0 ± 2.0 | ~60 mW | N/A | 31 GHz | MA [2] |
| 0.1–18 GHz | 9.5 ± 0.5 | ~144 mW | 11 dBm @ 14 | 40 GHz | DFA* [3] |
| 2–19 GHz | 9.6 ± 0.9 | ~200 mW | 11 dBm @ 19 | 30 GHz | MA |

* Darlington Feedback Amplifier.

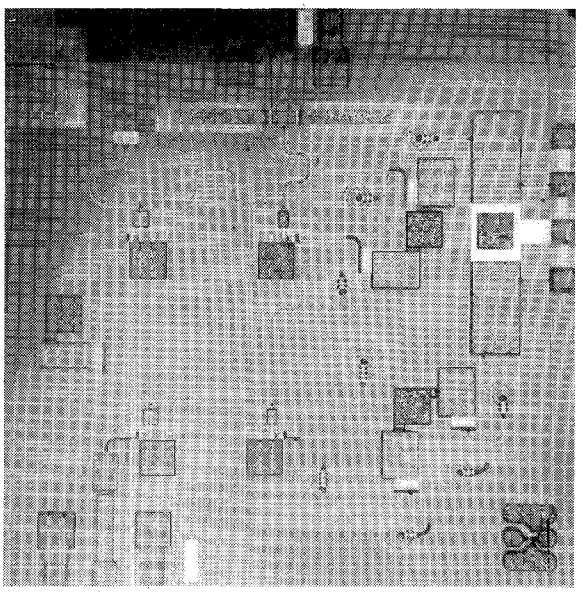

Fig. 2. Photograph of the monolithic HBT matrix amplifier.

HBT amplifier. Table I summarizes the key performance and device parameters of the present amplifier in addition to the amplifier reported in [1]–[3]. The measured noise figure of the presented MA varies from 16.2 dB at 2 GHz to 8.2 dB at 19 GHz with a minimum of 7.5 dB at 17 GHz. We processed four wafers with a RF circuit yield of more than 60%. The circuit demonstrated repeatable performance for all the chips that were tested. Compared to the GaAs MESFET wide-band monolithic matrix amplifiers [6], [7], the HBT matrix amplifier requires lower dc power for similar 1-dB compression and $IP_3$ performances.

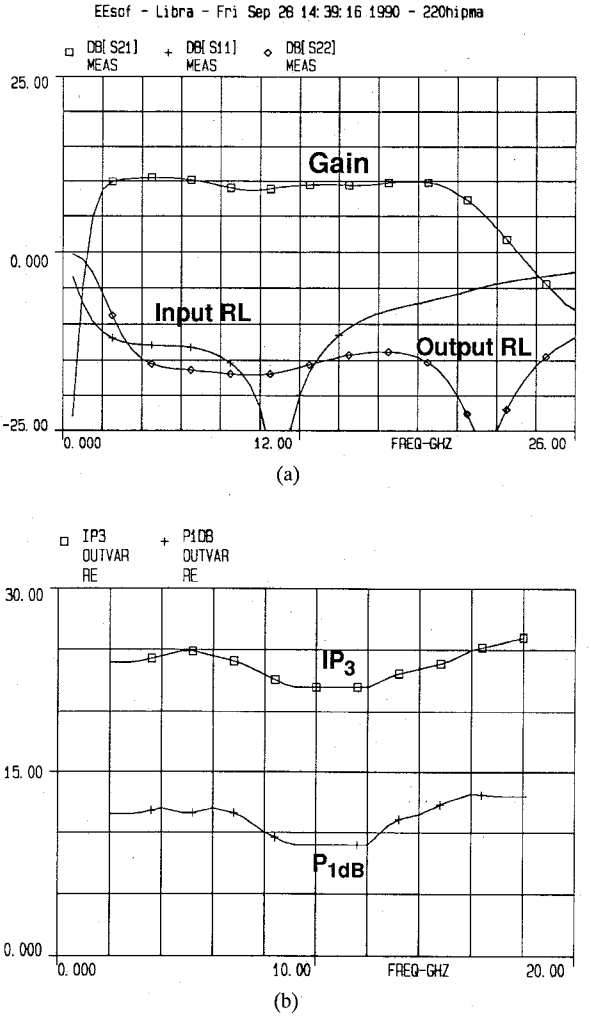


Fig. 3. (a) Measured gain, and input and output return losses of the matrix amplifier. (b) Measured $IP_3$ and 1 dB compression point of the matrix amplifier.

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